analog dialogue

A forum for the exchange of circuit technology: Analog and Digital, Monolithic and Discrete

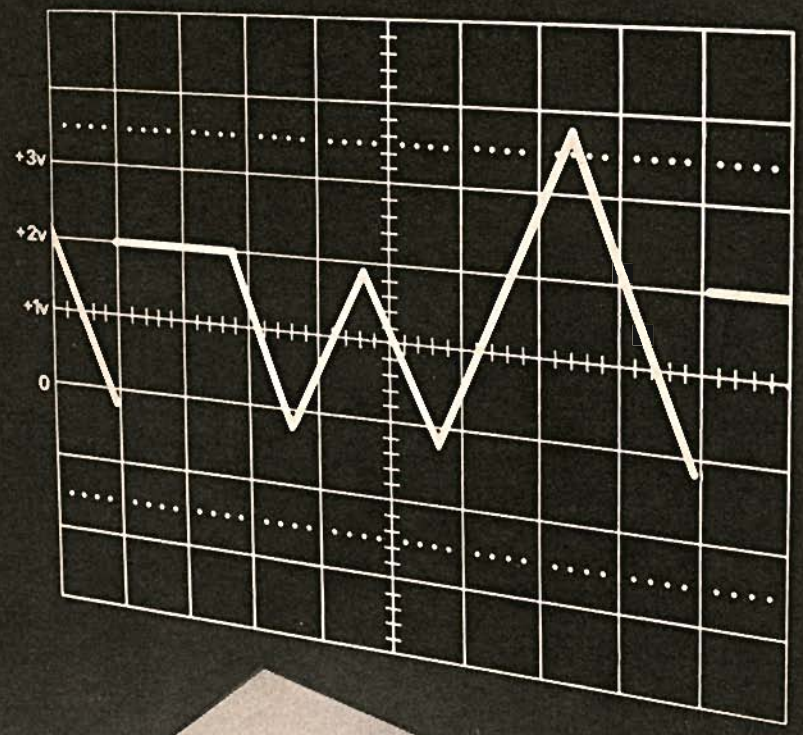
13-BIT MONOLITHIC CMOS A/D CONVERTER (page 3)

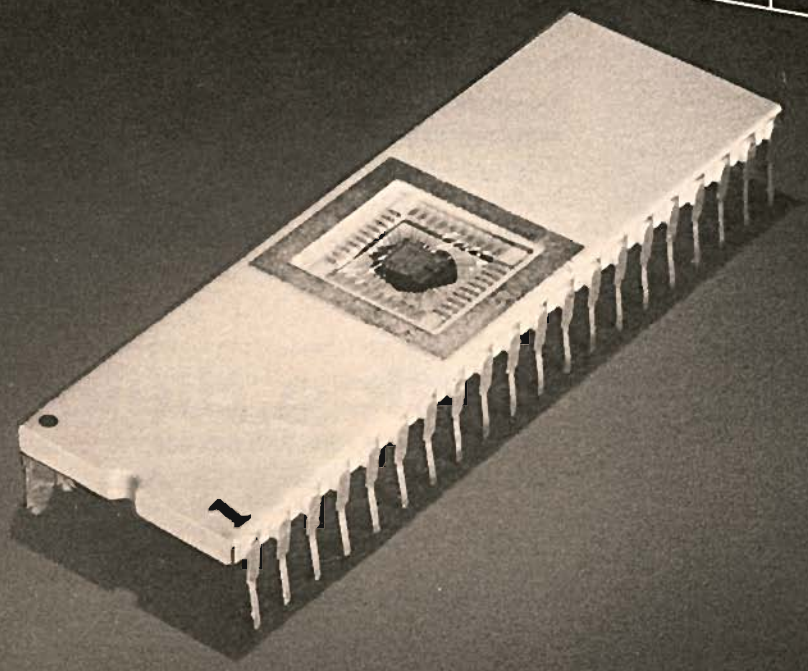
Also in this issue:

Monolithic Sample-Hold Amplifiers

FET-Input IC Electrometers

Full contents on page 3





Volume 10, No. 1, 1976

ANALOG DEVICES

Editor's Notes

DECENNIAL

Our first ten years in business having been weathered, it is perhaps appropriate to assess the late decade, one in which Analog Devices has appeared on the scene, survived, and prospered. As is our wont, as well as our charter, we shall hew here to technical matters; readers seeking further enlightenment on our business as a whole – present, prospective, and retrospective – are invited to request copies of the 1975 Annual Report, the President's message at our Annual Meeting, and the not-unpleasant tidings in the 1976 first-quarter Report.

For this *ith* recital of our history, we hope for the indulgence of our faithful readers on the ground – established by our recent survey – that perhaps one-half of our present readers have been with us for two years or less.

For the first third of the decade, our activities were fully consonant with our corporate name – we developed and produced high-performance modular operational amplifiers of all descriptions: FET-input, chopper, high-speed, parametric – and taught users how to apply them to best advantage. Despite the parallel growth of commodity IC's, our amplifier activities succeeded, because our amplifiers, backed in depth by applications information, helped solve user problems, aided and abetted by other Analog modules: multipliers, logarithmic devices, instrumentation amplifiers, and (the necessary) power supplies.

In the late sixties – the second third of our decade – we recognized that the destination of the information processed by our modules would increasingly be an interface with digital processing equipment. We also recognized that the cost and size advantages of IC's and hybrids would inevitably result in their encroachment upon (to begin with) the simple functions then available in modular form and would make possible more-complex modules, which would themselves be challenged, in an endless cycle reminiscent of the familiar picture of large fish eating smaller fish eating smaller fish, etc. – but in a reversed progression.

For A/D and D/A converters, the manifestation of progress was the replacement of breadbox-sized converters by modules of ever-increasing speed and accuracy and ever-decreasing size and cost. For analog functions, we established an integrated-circuit facility that initially concentrated on high-performance op amps, multipliers, and converter quad-switches.

In the final third of the decade, we articulated the mission of Analog Devices, the unifying underpinning of our technical activities – the key to both past and future. Succinctly stated, it is: *to design and produce innovative electronic products that acquire, convert, condition, or display data for precision measurement and control.*

In an explosion of progress, there appeared: digital panel meters, SERDEX (SERial Data-EXchange) products, and denier sensors and systems for the textile industry; low-cost modular converters, including V/f's; rms modules; high-performance multiplier-dividers and functional modules; microprocessor-compatible IC A/D and D/A converters; precision resistor networks; and a host of other precision IC's: voltage references, instrumentation amplifiers, multiplier-dividers, and op amps.

The keys to our future lie in the statement of our mission and in a disposition and a competence to seek out and understand the user's problems and to provide him with helpful solutions.

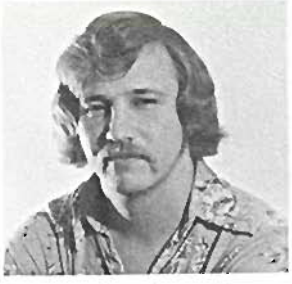
In the first decade, the technologies we used resulted principally in products of small size that performed simple unit functions. While efforts in that product area will continue and intensify, the second decade will – almost from the outset – see the introduction of more-complex products of greater size and scope. A salient feature of the new system-oriented products will be their advanced *software*. Provided as an inherent necessity, it will make life easier for the user, in much the same way that ADI's traditional diversity and abundance of publications helped (and will continue to help) component users.

The first ten years were fun – but as nothing compared to the next ten!

▶▶▶

Dan Sheingold

THE AUTHORS



Will Ritmanich (page 3), Applications Engineer at Analog Devices Microsystems, obtained his basic engineering background at Foothill College. Prior to joining ADI, he spent time in the U.S. Navy, then at National Semiconductor, Fairchild Semiconductor, and American Microsystems, where he was responsible for product engineering and test engineering for various linear and MOS integrated-circuit products.

Dennis Langley (page 3) is Project Engineer at Analog Devices Microsystems and was responsible for development of the AD7550. Before joining ADI, Dennis designed modular conversion products for Cycon and Zeltex and was Product Engineer at Fairchild Semiconductor. He has a B.S. from the University of Illinois and has completed course work for the M.S. degree at U.C. Berkeley.

(more Authors on page 18)

analog dialogue

Route 1 Industrial Park, P.O. Box 280, Norwood, Mass. 02062

Published by Analog Devices, Inc., and available at no charge to engineers and scientists who use or think about I.C. or discrete analog, conversion, data handling and display circuits. Correspondence is welcome and should be addressed to Editor, *Analog Dialogue*, P.O. Box 280, Norwood, Massachusetts, U.S.A. 02062. Analog Devices, Inc., has representatives and sales offices throughout the world. For information regarding our products and their applications, you are invited to use the enclosed Business Reply card, write to the above address, or phone 617-329-4700, TWX 710-394-6577, Telex 924 491, or cable ANALOG NORWOOD MASS.

13-BIT MONOLITHIC CMOS A/D CONVERTER

AD7550 Has 1ppm/°C Gain and Offset Sensitivities, 3-State Logic, Two's-Complement Output

by Will Ritmanich, Dennis Langley, and Ivar Wold

The AD7550* is a 13-Bit A/D Converter on a single 3 x 3.2mm (118 x 125 mil) chip, enclosed in a 40-pin dual in-line package (Figure 1). It utilizes a totally-new "Quad-Slope" integration technique†, which provides both autozeroing and low sensitivity to component error, supply variations, and temperature changes. It accepts analog inputs of either polarity; the output is available as either a train of pulses for external counting, or as a parallel 2's-complement word, divided into 5- and 8-bit bytes, and buffered by 3-state logic especially suited for microprocessor-controlled bus-oriented systems. The AD7550 interfaces directly with either TTL or CMOS logic.

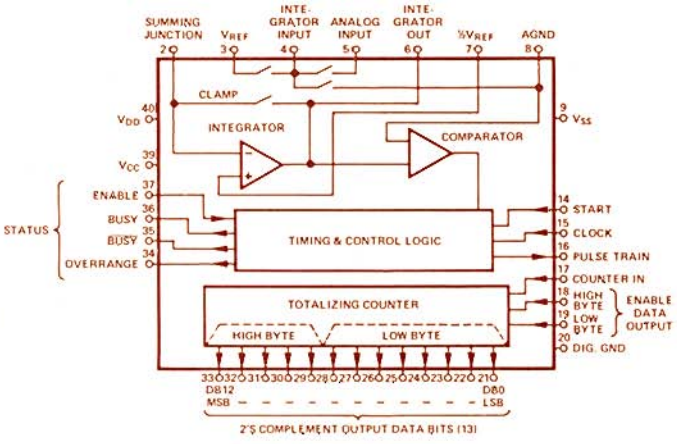


Figure 1. Block diagram of the AD7550 A/D converter.

Requiring typically only 8mW total power (V_{DD} = 12V, V_{SS} = 0 to -5V, and V_{CC} = 5V up to V_{DD}), and a single external positive reference, the AD7550 contains its own comparator, integrating amplifier, clock, control-, counting-, and buffer logic, and analog switches. Since the reference is applied externally, the AD7550 may be used for ratiometric conversion. The internal clock may be overriden by an external clock for applications in which an external clock is desirable. The only passive external components normally required are a resistive divider-pair for the reference and a resistor-capacitor pair for the integrator (Figure 2).

Because of the integrating technique used (see page 5), the digital output is monotonic, with no missing codes. The AD7550 will accurately digitize signals from up to slightly less than one-half the maximum reference down to levels limited only by the internal FET-input amplifier's ability to accurately integrate small microvolt-level signals without errors due to noise. Because the Quad-Slope integration technique accurately adjusts for offsets over the temperature range, the zero-drift and gain-temperature coefficients are less than 1ppm/°C maximum, at typical conversion speeds of 40Hz, with ±½LSB differential nonlinearity. The AD7550BD is priced at $35 (1–49), $25 in hundreds.

*Use the reply card to request complete information on the AD7550.
†U.S. Patent 3,872,466

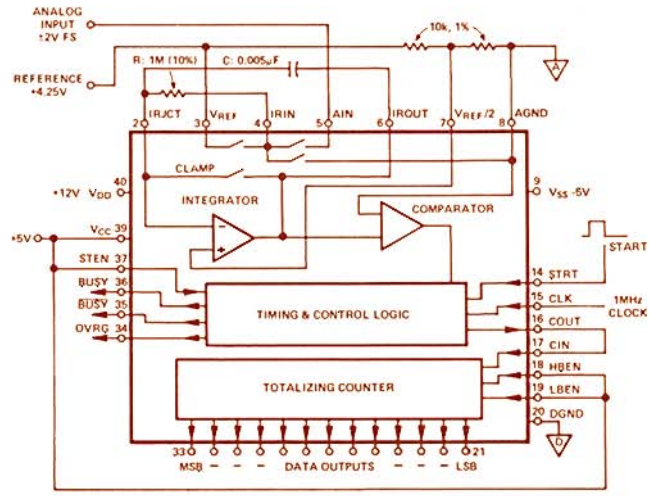


Figure 2. AD7550 connections for basic operation.

MICROPROCESSOR COMPATIBILITY

The AD7550 was specifically designed to be easy to use in data-bus systems, where its 3-state outputs are under external

(continued on the next page)

IN THIS ISSUE

Volume 10, Number 1, 1976, 20 pages

Editor's Notes, Authors 2
13-Bit Monolithic CMOS A/D Converter 3
Monolithic Sample-Hold Amplifiers 6
Inductosyn-to-Digital Converters 8
10 Volt (±1mV) References 10
FET-Input IC Electrometers 11
New Products:
Low-Cost Chopper 12
6-Decade Log-Ratio 12
100kHz V/f Converter 12
Three More "2nd-Generation" DPM's 13
Application Briefs:
Simple Rules for Choosing Resistor Values in Adder-Subtractor Circuits 14
D/A Conversion with Single-Supply Circuit 15
Differential High-Impedance rms-to-dc Conversion . . 15
Audio Application Ideas for CMOS DAC's 16
Potpourri: More Authors, HP-25 Resistance-Computation Program for Adder-Subtractor Circuits, etc. 18
Worth Reading: Book Review (*Operational Amplifiers* – Roberge), Last Issue of *Analog Dialogue*, Erratum . . 19
Advertisement: Digital Panel Meters. . . . . Back Cover

control. In this respect, the timing-sequencing and data-bus connections are compatible with those of the earlier AD7570* 10-bit successive-approximation A/D converter and the AD7522* multiplying D/A converter.

- The positive-true parallel data outputs (bits 0–12), the overrange indication, and the conversion status lines (BUSY, $\overline{\text{BUSY}}$) are 3-state and are isolated from the common data bus until appropriate interrogation signals are received (Data ready? High byte? Low byte?)

- The five most-significant bits (including the sign bit), the 8 least-significant bits, and the three status bits can be interrogated in separate bytes; all 13 bits can be furnished on an 8-bit common data-bus in 2 bytes.

- The serial-output pulse stream is brought out on a separate pin with regular (TTL or CMOS) logic levels; this permits the data to be manipulated before being clocked into the output buffers. The pulse train, C_{OUT}, is activated after the completion of the measurement cycle and has:

$$C_{OUT} = \left[\frac{2.125V_{IN}}{V_{REF}} + 1\right] (4096) \text{ counts}$$

- If the control inputs are connected to the appropriate logic levels, the AD7550 will work as a conventional 13-bit parallel-binary A/D converter.

APPLICATIONS

The AD7550's *forte* lies in applications for which accuracy and lack of discontinuities (such as missed codes), especially over wide temperature ranges, are vastly more important than speed of conversion. The self-contained nature of the AD7550, its low power consumption, and its insensitivity to temperature and supply voltage make it ideal for use in compact, remote, battery-powered precision instrumentation, for example, in seismic or geological exploration. On the other hand, its special control features allow it to be readily employed in microprocessor-controlled data-acquisition systems where 13-bit accuracy, flexible polarity, and a noise-averaging capability are necessary and high speed isn't.

Panel-meter and digital-voltmeter applications, especially in conjunction with a requirement for binary data for system use, and where high accuracy at elevated temperatures is necessary, are also pregnant possibilities. The count-out/count-in feature permits the pulse count to be manipulated separately (for auxiliary BCD displays), or prior to being counted in the tri-state-buffered counter (for example, by the use of binary rate-multipliers).

Figure 2 shows the basic circuit connection for binary operation. With all the data-output command inputs held high, as shown, parallel data will be present at the outputs. By selectively exercising the various command inputs, HBEN (High Byte ENable: 5 most-significant bits), LBEN (Low Byte ENable: 8 least-significant bits), and STEN (STatus ENable: OVer RanGe, BUSY, $\overline{\text{BUSY}}$), the desired data can be made available on an 8-bit data bus. The internal clock can be employed simply by replacing the 1MHz clock-input lead by a capacitor from the CLocK terminal to ground. Similarly, repetitive auto-start can be gained by connecting a capacitor from the STaRT terminal to ground.

*For information on these devices, use the reply card.

SINGLE-SUPPLY OPERATION

Figure 3 illustrates operation from a single +15V power supply. The AGND (Analog GrouND) terminal is biased to a positive voltage (relative to the converter power supply), which offsets the AD7550 transfer function. If the voltage at AGND is exactly one-half full-scale input (unipolar positive) and the reference is at 1.5625 the full-scale input, the negative full-scale input voltage is shifted to occur precisely at 0V.

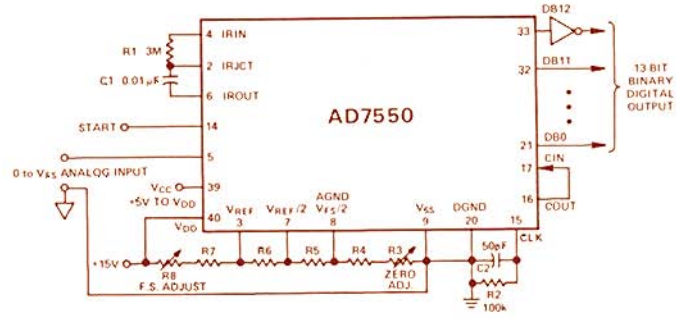


Figure 3. AD7550 single-supply operation (13-bit binary).

The adjustable resistors permit the zero and full-scale points to be fine-trimmed. Since drifts in the resistance ladder or the power-supply voltage directly affect the reference, they will directly affect the scale factor and the offset, but not the mid-scale point. Since the circuit provides *unipolar* 13-bit conversion, the normal 2's-complement code (used for bipolar conversion) is easily changed to straight binary by complementing DB12. The digital inputs and outputs are CMOS-compatible; although not shown, the control inputs should be tied to V_{CC}. If the AD7550, used in this configuration with sensing transducers, shares their power supply, the ratiometric transfer characteristics of the AD7550 will tend to reject supply-voltage variations.

3½-DIGIT DPM (0 TO +2V FULL SCALE)

Figure 4 shows a simple circuit to provide 3½-digit readout for positive input voltages. The number of output pulses is divided by 2, and the reference is scaled so that 1999 of the 2047 output pulses clock a National MM74C928 counter-latch-display through a 0 to +1.999V range.

An AD580* 2.5V reference and an AD301AL* op amp provide the reference voltage, adjustable by the 500Ω resistor.

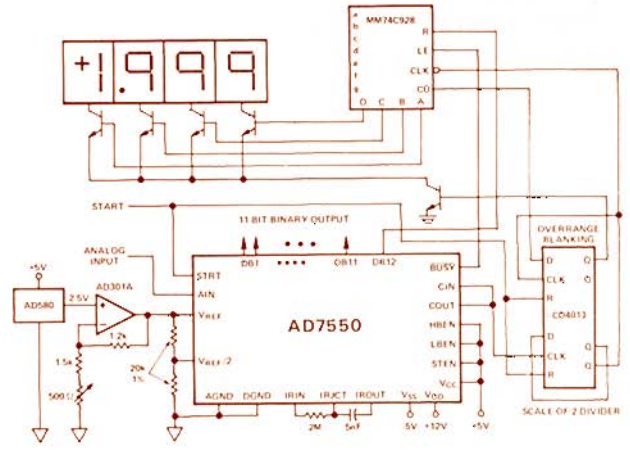


Figure 4. 3½-digit display application.

*For information on these products, use the reply card.

Conversion begins when the STaRT command is initiated. When DB12 goes low, indicating a positive input, the MM74C928 starts its count, corresponding to the analog input voltage. After the last C_{OUT} pulse, $\overline{BUSY}$ goes high and latches the display. The Carry output of the MM74C928 indicates overrange by toggling the CD4013 to blank the display for inputs $\geq$2.000V.

HOW THE QUAD-SLOPE CONVERTER WORKS

The quad-slope converter is an integrator-counter converter, related to the conventional dual-slope converter. However, it includes two additional integration phases for virtual cancellation of offset- and scale-factor errors. Its operation can be seen in Figure 5.

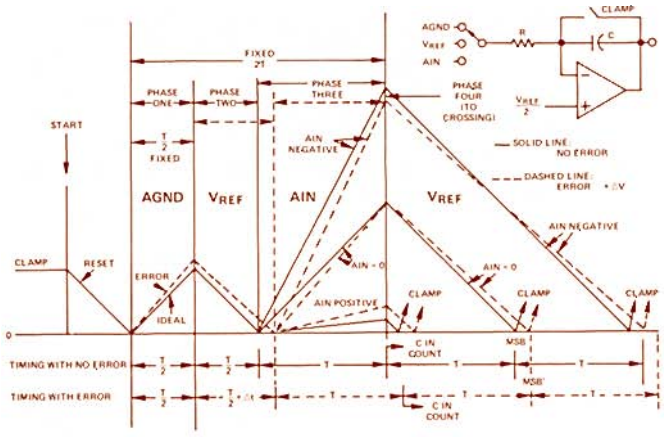


Figure 5. Illustration of quad-slope principle: integrator output waveforms for positive, negative, and zero input – with and without error.

The integrator has four modes of connection, determined by internally-controlled CMOS switch settings: Clamped (when no conversion is in process), Grounded input, Reference input, and Analog (signal) input. The positive input of the integrating amplifier is continuously connected to $V_{REF}/2$. When a conversion is initiated (phase "0"), V_{REF} is applied to the integrator input, providing a net positive voltage, $V_{REF} - V_{REF}/2$, across the integrator's input resistor, resulting in a negative-going ramp at the output. When the output is equal to the comparator trip-voltage, phase 1 is initiated.

Phase 1. The integrator input is connected to Analog Ground. Since the integrating resistor has a net negative voltage across it, equal to $-V_{REF}/2$, plus any error, the output increases positively at a proportional rate. At the beginning of Phase 1, a counter starts counting clock pulses. When it has counted a number of pulses representing an interval, T/2, Phase 2 is initiated; the counter continues to count.

Phase 2. The integrator input is connected to the Reference. Since the voltage across the integrating resistor is $+V_{REF}/2$, plus any error, the output ramps down at a proportional rate. When the output reaches the comparator trip voltage, Phase 3 is initiated. If there were no error, the time for Phase 2 would be equal to T/2, the same as for Phase 1. Any error will increase or decrease the time to the trip point by an amount Δt. Note that the trip point is approached with the same slope and from the same direction as at the end of Phase 0 (and also the end of Phase 4), hence any comparator hysteresis errors and differential propagation delays are avoided.

Phase 3. The integrator input is connected to the Analog signal, which is positive or negative, and less than $V_{REF}/2$ in magnitude. The net input to the integrator will always be negative and equal to $A_{IN} - V_{REF}/2$, plus any error. The output of the integrator will ramp upwards with a proportional slope. For large positive inputs, the output slope will be small; for large negative inputs, the output slope will be steep; and for zero input, the slope will be the same as in Phase 1. Phase 3 is terminated when the counter that started at the beginning of Phase 1 reaches a count corresponding to 2T.

Because Phases 1, 2, and 3 occupy a total period 2T, Phase 3 is lengthened or shortened by Δt, the same amount by which Phase 2 was shortened or lengthened. At the *beginning* of Phase 3, a second counter is started, counting *down* from zero*; note that, with zero error, it starts at T exactly; but with an error, it starts at $T \pm \Delta t$.

Phase 4. The integrator input is again connected to the Reference, and it ramps down at the rate $V_{REF}/2$, plus any error. Phase 4 ends when the integrator output reaches the trip point, after which the integrator is clamped and the second counter is stopped. Conversion is now complete, and the counter output is a 2's complement representation of the analog input.

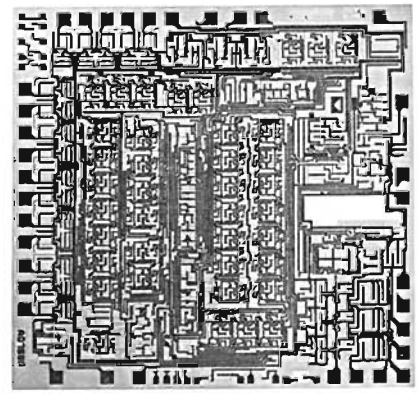
Discussion. The data sheet describes the actual workings of the circuit in some detail and includes a derivation of the error equation. Here we will rely somewhat more on graphics and intuition to show that it actually works. In Figure 5, it can be seen that the time from the MSB crossing, corresponding to zero input, to the time of occurrence of the crossing corresponding to a positive or a negative input, is proportional to that input. The effect of an error is simply to shift *all* crossings by an equal amount of time, Δt.

If the counter's capacity is 2T, and if it counts down from all zero's at the beginning of Phase 3, then at the largest positive number, it will read 0 1111 1111 1111 (and will stop there if a crossing occurs), at zero it will read 0 0000 0000 0000, and at the largest negative number, it will read 1 0000 0000 0001, a range which will be recognized as belonging to a 2's-complement code.

In actual practice, in order to avoid negative integration and allow sufficient time after Phase 4 begins for offset correction and overrange indication, a somewhat different counting scheme is used, in association with an input full-scale range of $V_{REF}/2.125$, instead of $V_{REF}/2$.

▶▶▶

*The implementation discussed here is simplified for clarity.



MONOLITHIC SAMPLE-HOLD AMPLIFIERS

2 New Devices Achieve 12-Bit Performance, Low Cost of AD582KH May End "Do-It-Yourself" Lashups

by Dave Kress and Dick Wagner

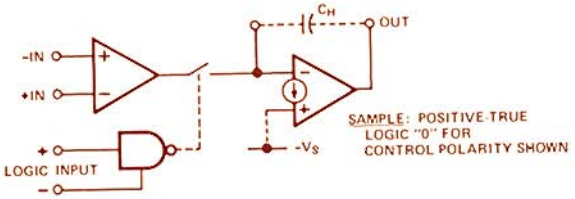
The AD582* and AD583* are two new monolithic integrated-circuit sample-hold amplifiers. Both are self-contained, except for the externally-connected *hold* capacitor, C_H, which is chosen by the user for the best compromise between speed of acquisition-and-tracking, and error magnitudes in *hold*.

The AD583 provides extremely-fast acquisition (2μs to 0.1% with C_H = 100pF, 10μs to 0.01% with 1000pF), low aperture time (50ns), and a fast 5V/μs slewing rate (C_H = 1000pF). The AD582, while somewhat slower (6μs to 0.1% with 100pF, 25μs to 0.01% with 1000pF), is far less costly, $5.95 in 100's, $8.90 (1–24) for AD582KH, vs. $14.85 in 100's, $20.25 (1–24) for AD583KD.

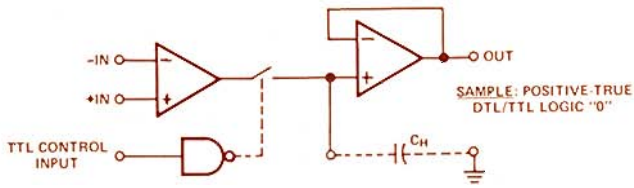
Besides having lower cost, the AD582 is also capable of greater accuracy, with a maximum charge transfer of 5pC (5mV at 1000pF), compared to 20pC (20mV at 1000pF) for the AD583, when switched from *sample* to *hold*. Minimum error with the optimum value of C_H is also considerably less: 500μV at C_H = 3000pF, vs. 2mV with C_H = 5000pF.

Sample-holds are conventionally used in data-acquisition systems, either to "freeze" fast-moving signals during conversion, or to store multiplexer outputs while the signal is being converted and the multiplexer is seeking the next signal to be converted. In analog data-reduction, sample-holds may be used to determine peaks or valleys and to facilitate analog computations involving signals obtained at different instants of time. Other uses include automatic zero-correction systems and spike-noise eliminators ("deglitchers").†

The AD582 and AD583 both have differential inputs; they both utilize high gain in a feedback loop for rapid tracking.



(a) AD582 has differential logic inputs, current switching, output integrator.

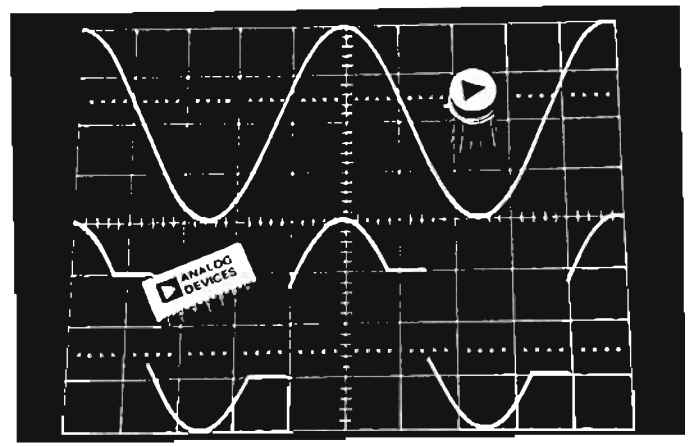


(b) AD583 has single-polarity logic, output follower.

Figure 1. Block diagrams of the AD582 and AD583.

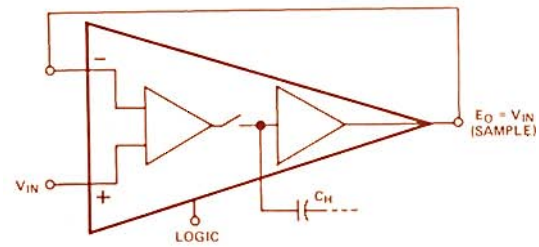
*For technical data on these devices, use the reply card.

†Considerable information on the nature and uses of sample-holds can be found in the *Analog-Digital Conversion Handbook*, available from Analog Devices @ $3.95.

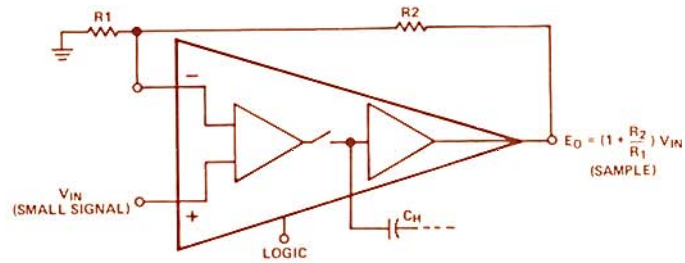


However, there are several differences, as shown in Figure 1. The AD582's *hold* capacitor is connected as the feedback element of an integrator; the AD583's *hold* capacitor is unloaded by a unity-gain follower. While the AD583's control input accepts only positive-true 5V TTL, the differential control input of the AD582 permits easy interfacing to any standard logic family – TTL, DTL, 3-, 5-, or 15-volt CMOS, 15V HTL, with either positive- or negative-true sense. The AD583 has a lower output impedance in *hold*, for applications in which the load on the sample-hold amplifier is variable.

Both devices perform essentially as differential operational amplifiers with open-loop dc gain of 25,000 in the *sample* (or *track*) mode; their dynamics depend on the value of C_H. They can therefore be used either as high-impedance gain-of-one followers with normalized input signals, or to obtain single-ended or differential gain for low-level inputs (Figure 2). In



(a) Conventional unity-gain follower application.



(b) Follower with gain.

Figure 2. Basic sample-hold follower circuits.

either case, when a *hold* signal is applied to the control input, the output is ideally held at the last value until the device is returned to *sample*.

Sample-holds are by no means ideal devices, but they are sufficiently ideal for many applications. They can be best applied if the essential sources of error are commonly understood and are adequately characterized (and/or specified) by manufacturers. Since there is no industry approach, it may be useful to provide a brief review of terminology used in relation to Analog Devices integrated-circuit sample-hold amplifiers.

Figure 3 shows the common sources of error that occur during the four phases of operation, and Figure 4 shows how some of them are affected by the magnitude of C_H. In the adjacent column will be found a discussion of sample-hold parameters. The four phases of operation are:

- *Sample*: The output is seeking to track the input, with the relationship determined by the external feedback connections, as an operational amplifier. Error sources include bandwidth and slewing rate limitations (a function of C_H), low-frequency gain errors, and dc offset.
- *Sample-to-Hold*: When the control signal switches, the S-H output should simply stop changing, and hold the last value. In fact, there will be aperture-time and settling-time errors, during which delays, spikes, and lags occur, and a sample-hold offset, caused by coupled charge from the control signal.
- *Hold*: The output should stay put. Actually, it will "droop" up or down as a function of C_H and the leakage current through it, and ac input signals will "feed through" to the output.

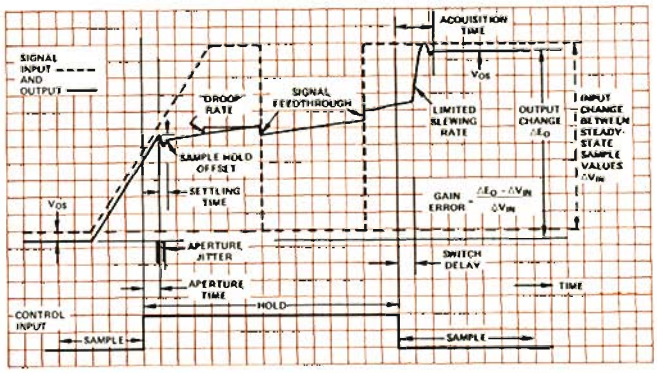


Figure 3. Principal sample/hold dynamic parameters. Errors are exaggerated for clarity.

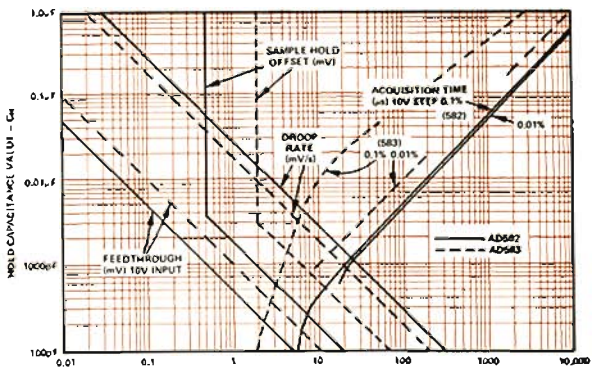


Figure 4. Circuit parameters as a function of hold capacitance.

- *Hold-to-Sample*: When the control signal switches, the output should immediately jump to the existing input value and follow it accurately thereafter. In real devices, there will be switching-delay, acquisition-time, and settling-time errors.

PARAMETERS OF SAMPLE-HOLD AMPLIFIERS

Sample Mode

Gain errors may be expressed in terms of *scale factor*, *nonlinearity*, or both. In the case of differential-input devices, such as the AD582 and AD583, the limiting factor in the unity-gain follower is the *input common-mode error* and its nonlinearity (0.01% max for AD582, 0.02% typ for AD583), rather than the *dc open-loop gain* of 25,000. When feasible, the unity gain inverter configuration will provide the best linearity and gain accuracy.

"Op-amp errors" are those errors that generally apply to op amps, whether or not they are gated; they include *offset voltage*, *bias current*, their sensitivities to temperature and supply voltage, etc. Dynamic op-amp errors which involve *slewing* and/or *gain-bandwidth*, will depend on the value of C_H.

Sample-to-Hold Transition

Aperture time is the time from the *hold* command until the hold capacitor is actually disconnected. If the time were fixed, the command could be advanced sufficiently to obtain a switch opening (and subsequent "freezing" of the data) at exactly the right time. However, it can differ by 20% or more from unit to unit and is subject to *"jitter"* which is the ultimate determinant of uncertainty of the time of measurement.

From the opening of the switch, the *settling time* is the interval required for the output to settle to its final value, within a given percentage of full scale. In data acquisition, it is a critical parameter, because an A-D converter should not begin conversion until this interval is complete.

Sample-to-hold offset is a step produced by charge coupled from the logic signal to the *hold* capacitor *via* stray capacitance and internal operating-point changes. This step can be reduced up to a point by increasing the magnitude of C_H. It can be further reduced by "charge cancellation" circuitry, which is most-successfully employed if the S-H offset is small to begin with, as in the AD582.

Hold Mode

Droop is simply the integration of net positive or negative leakage current in the *hold* capacitor and is inversely proportional to C_H: $dV/dt = I/C_H$. For example, a droop specification of 50mV/s with C_H = 1000pF at +25°C indicates a leakage current of 50pA.

Feedthrough is the residue of an ac input signal that is coupled into the *hold* capacitor by stray capacitance or leakage across the switch. It is inversely proportional to C_H.

Hold-to-Sample Transition

Acquisition time is the shortest time after a *sample* command has been given that a *hold* command can be given and result in retaining a voltage acquired with the necessary accuracy. For devices of the nature of the AD582 and AD583, involving the kind of causality found in high-gain feedback loops, it is equal to the time interval for the switch to close and the output to slew and settle to within the prescribed limits.

▶▶▶

INDUCTOSYN-TO-DIGITAL CONVERTERS

For the Accurate Measurement of Displacement; Their Use in Linear Measurements for Control Systems

by D. McDonnell

With the coming of computer control of machine tools and drafting systems, the need arose for a linear measurement system that could work with digital data that was fed from the computer-controller. Optically-encoded discs at the end of leadscrews, Moiré-fringe techniques using optical gratings along the machine bed, and other such devices have been used, including lasers, in applications for which they were suitable. However, none of these devices has the combination of ruggedness and low cost of the Farrand Linear Inductosyn.

Until recently, the use of the Inductosyn with digital-control systems has been limited by the lack of high-speed methods of accurately interpolating within one period of the scale. The high-speed tracking Inductosyn-to-Digital converter provides an elegant solution to this problem. The Analog Devices IDC1701 and IDC1703 are converters* specifically designed for this purpose.

THE INDUCTOSYN

For machine-tool and other control systems, the use of the Farrand Linear Inductosyn† has been recognized for many years as an accurate method for performing linear measurements. Inductosyns are manufactured in forms suitable for measuring either straight-line distances or angles. Here we consider the use of linear Inductosyn measurements, though nearly all aspects of the discussion can be easily applied for rotary measurements.

The linear Inductosyn is an especially-useful tool in the high-resolution measurement and control of linear motion over relatively-large distances (many meters). It consists of two magnetically-coupled parts, one usually fixed to the bed of a machine, the other movable with the tools or work. The fixed portion consists of joined lengths of material with a printed rectangular "square-wave" pattern; the movable portion has two short lengths of the same pattern, displaced by one-quarter period ("90°"). The two parts which form the Inductosyn are shown in principle in Figure 1. The fixed "ruler" is typically

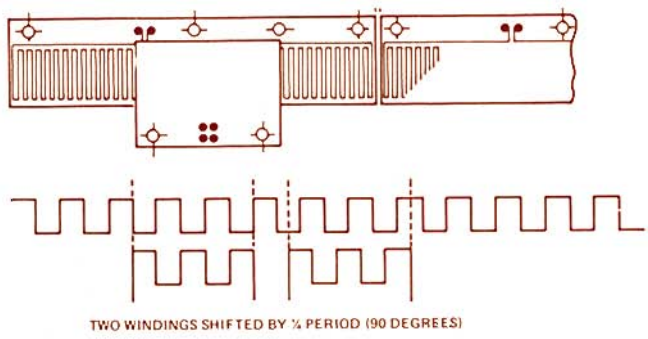


Figure 1. The Inductosyn track and slider system.

available in either 10" or 250mm lengths, depending on whether the metric or the English scale is to be used. (The fixed scales are also available as continuous strip in lengths up to 30 feet – 9.144m.)

Like the two-phase synchro resolver, the Inductosyn utilizes the inductive coupling between a reference winding and two mutually-orthogonal windings to provide an output that is a function of position. In the Inductosyn, the electromagnetic circuits are rearranged in two parallel flat plates, with an intervening electrostatic shield to minimize capacitive coupling. The Inductosyn is a bilateral device; that is, either (1) the fixed winding can be driven by an ac reference, with the slider position manifested in the relative amplitudes of the voltages induced in the two orthogonal windings, or (2) the two windings could be driven by orthogonal resolver outputs, with the fixed winding providing a measure of the difference between the resolver angle and the corresponding positional displacement of the slider.

The second mode of operation is used in conventional Inductosyn feedback-control systems, with the slider driven to maintain nil error between the "set point", applied by the resolver, and the incremental slider position (within a given modulus (cycle) of the printed stator). Although effective in analog servo systems, (2) is not as useful as (1) in digitally-controlled systems. Our discussion in these pages will deal with applications of the first alternative.

INDUCTOSYN-TO-DIGITAL CONVERSION SYSTEMS

The reference input to the fixed scale is an ac current generator at a frequency typically greater than 2.5kHz. The ac outputs at the slider windings, with amplitudes respectively proportional to the sine and cosine of the incremental angle, are preamplified and applied to the input of an Inductosyn-to-Digital Converter (IDC). A reference ac signal, in a phase relationship with the current input to the stator, is also fed into the converter, as shown in Figure 2. As the slider of the Inductosyn is moved through one cycle of the pattern, the

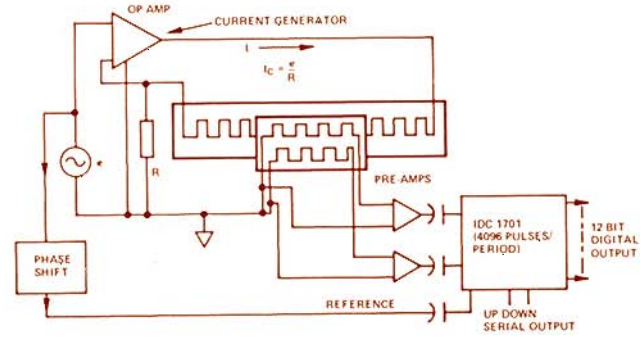


Figure 2. The Inductosyn as a resolver control transformer with digital output.

*Use the reply card to request information on these devices.

†Farrand, Inc. trademark

digital output of the IDC will change through 360°. For absolute positioning, relative to a datum, a counter counts half cycles, providing the most-significant bits of information, and the IDC provides the fractional information, at resolutions up to 12 bits. The outstanding degree of resolution available is quite apparent. A typical system is shown in Figure 3.

PERFORMANCE REQUIREMENT FOR THE IDC

For modern milling and drafting machines, the speed of operation is very important. A standard minimum top speed of 10 meters/minute is now accepted as being necessary in machine-tool control. The standard pitch of the Inductosyns being used is 2.0mm. Since one revolution corresponds to 2.0mm along the track, the top speed is equivalent to 83.3 revolutions per second.

For some standard European machines, a reading rate of 40 commands (or readings) per second has been adopted – providing an interval of 25ms between readings. This means that at the maximum speed, the machine will have moved by 2.08 periods between samples. This means, further, that the IDC must have two extra up-down counting stages beyond the normal MSB of 180°, or else lost periods will occur at high speed.

In addition, the IDC should be capable of following accelerations of up to 1500 revolutions/second/second more or less accurately but without saturating the error detector. This acceleration rate implies that the machine can get up to its maximum velocity of 10 meters/minute in approximately 5mm displacement; similarly, it can be brought to rest from its maximum speed in 5mm.

The choice of carrier frequency for use in the converter is a compromise, taking into account: (1) at *low* frequencies, the signals out of the Inductosyn are too small, in comparison to the amplifier input noise and system interference; (2) at *high* frequencies, the capacitances across the precision resistors and switches establish the limiting speed. From the point-of-view of acceleration performance, the higher the frequency, the better, since less smoothing is needed in the shaping circuits following the phase-sensitive detector.

Two factors influence the useful maximum resolution: (1) the precision with which the induced voltages in the two windings follow the sine and cosine laws with angle and (2) the degree of smoothness of control required. The higher the resolution required, the more difficult it becomes to meet the maximum velocity and acceleration requirements. The maximum resolution that seems justified by the overall accuracy of the system is 12 bits for a 2mm period (1 bit corresponds to 0.5μm, or 19μin, with 1-bit smoothness.

The IDC1701 and IDC1703 are tracking Inductosyn-to-digital converters which have been specifically designed to meet the needs of Inductosyn systems. They differ from other tracking resolver-to-digital converters principally in having the ability to track at 150 pitches/second and accelerate at 250/second/second with only 1LSB error. They are designed to work with carrier frequencies from 2kHz to 10kHz, and are tested at 5kHz. They accept input signals of ¼V rms, and provide digital outputs at TTL levels. Because of the low levels and high-resolution capability, the input signal amplifiers should be well-shielded and located as close to the slider as possible – preferably *on* the slider.

The stator is driven by current in order to obtain complete control over the flux generated in the stator, irrespective of differing track resistances in a series chain or tendencies by stray fields linking the track to induce parasitic currents.

The IDC1701 has parallel and serial (4096 pulses/pitch) digital outputs; the IDC1703 outputs are up-down pulses at 4000/pitch, together with carry-borrow pulses for each complete pitch. The latter is necessary to obtain a precision datum point. The price of either unit is $350 by the 1's.

▶▶▶

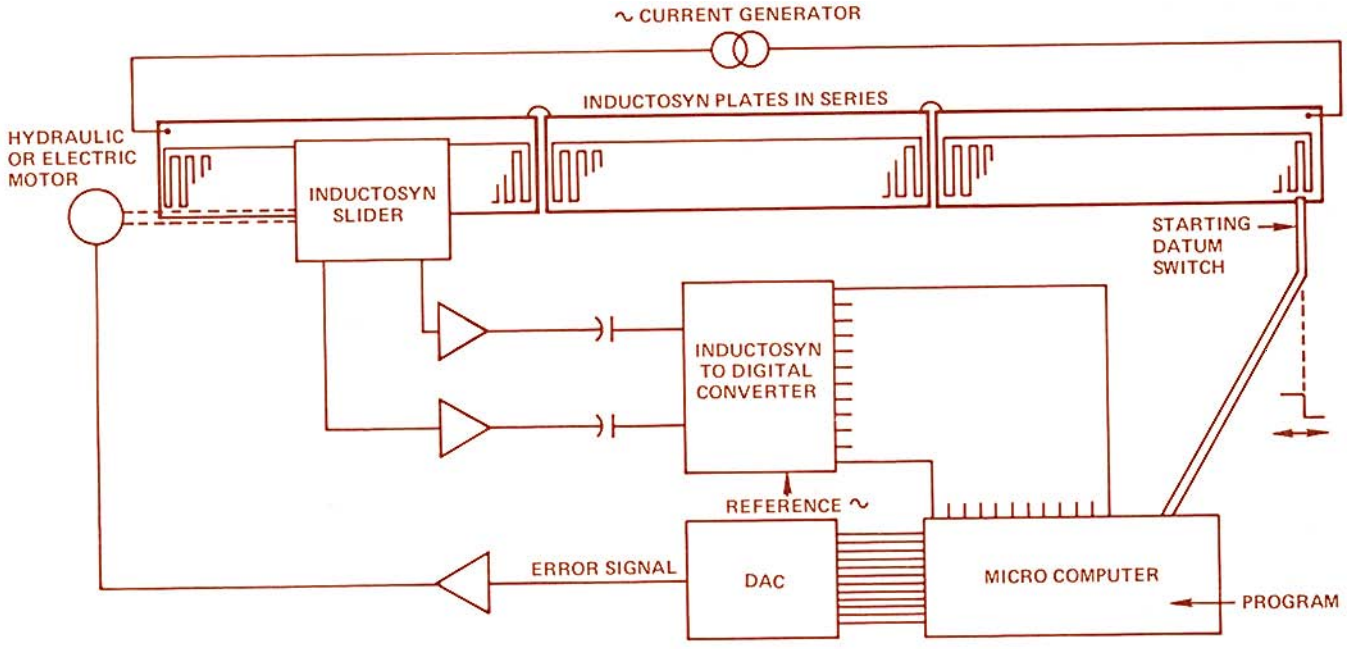


Figure 3. The use of an Inductosyn-to-digital converter in an Inductosyn control loop.

10-VOLT (±1mV) REFERENCES

Low-Cost Hybrids Have 5ppm/°C Stability
Choice Among +,–, or Both Polarities

by Jerry Gunn

In precision analog circuits, there is a recurring need for precisely-set, dependable reference voltages that can be used as a basis for introducing constant voltages or currents for bridge excitation, analog computation, predictable offsets and references, and A/D and D/A conversion. Some desirable properties of such references include:

- Accurate initial values (to within ±0.01%) to permit the use of fixed, predictable resistors, without tweaking
- Good stability over wide temperature ranges, comparable with that of typical precision resistors
- Ability to operate over a wide range of inputs – for example, ±20% of nominal – with regulation of only a few ppm/% of input variation
- Good load regulation. Although the loading on precision references is fixed in many circuits, load regulation still affects the initial value.
- Availability in a choice of polarities, including dual. Murphy's Law tells us that a single available reference is always of the wrong polarity, or may be insufficient, in any event, if several reference voltages are needed.

To meet these needs, 3 related references* are now available, for the popular 10.000V output level, all housed in hermetically-sealed 14-pin dual in-line packages: the AD2700 for +10V, the AD2701 for –10V, and the AD2702 for both polarities.

WHAT TYPICAL ALTERNATIVES EXIST?

- *If* the system power supply is sufficiently accurate, it can itself serve as a rather expensive reference.
- Operate a low-cost Zener diode at constant temperature; unload it with an op amp. This may prove bulky and unfeasible for very wide-temperature-range operation.
- Use a temperature-compensated band-gap reference, such as the 2.5V monolithic AD580† with appropriate op-amp circuitry (*Dialogue* 9-2). The result is not very compact, it requires a user tweak, and its best standard tempco is 10ppm/°C.
- Use a temperature-compensated Zener diode in a circuit like that of Figure 1 (which is the basic circuit of the AD2700 series). T-C Zeners are proven, have low noise and high stability. However, since the diode voltage is current-sensitive, the buffer must be used to unload the diode and reduce the influence of power-supply variations, as well as permit precise amplification from 6.2V (±5%) to 10.000V. In the AD2700 series, the circuit-design, assembly, test, and hermetic sealing in its DIP package are all provided, along with guaranteed performance, at a reasonably low cost ($10 in 100's for the AD2700L and AD2701L, $12 in 100's for the AD2702L dual reference).

*Use the reply card to request technical data on the AD2700/01/02 10V references.

†Use the reply card to request data on the AD580.

HOW IT WORKS

The high-gain operational amplifier serves to balance the bridge formed by R2 and the Zener diode, and R4 and R5. Since, at balance, $V_Z \cong (6.2/10)V_{OUT}$, $V_{OUT} \cong 10V$. The bridge ratio is laser-trimmed for $V_{OUT} = 10.000V$. Since $(V_{OUT} - V_Z)$ is nearly constant, irrespective of supply voltage, the variation of current through the diode is affected only to a second order by supply-voltage variations.

Resistor R1 facilitates startup and reduces the load current furnished by the amplifier, by supplying the 7.5mA diode current and part of the external load current, for $V_S = 15V$.

Because the circuit is a high-gain feedback loop, IR drops in the internal output leads and wirebonds can be compensated for by directly connecting the ends of measuring divider R4-R5 to the output pins. The resulting output resistance is 0.02Ω.

The AD2700/01/02 use the Analog Devices Ni-Cr-Au thin-film system (*Analog Dialogue*, 8-1, 8-2) for resistors and conductors, with a high-quality temperature-compensated reference diode and low-drift op-amp chip. To make best use of the stability of the reference diode, R4 and R5 – which determine the gain–track to better than 0.5ppm/°C, with low absolute temperature coefficients and excellent long-term stability.

PERFORMANCE

The device outputs are laser-trimmed at room temperature.‡ Their variation with changes in temperature is specified in terms of maximum total change at any temperature within the range (usually at the extremes). For example, the AD2700L is specified to have a maximum change of ±0.03% over the range -25°C to +85°C. The AD2700U has a maximum change of +0.03%, -0.05% over the range -55°C to +125°C.

The AD2700 series will operate with input voltages from +12V to a maximum of 20V, with overload tolerance of up to 40VDC for short periods. Input regulation is 5ppm/% ΔV_S. Quiescent power consumption is 160mW at 15V. The output, protected against short circuits, has a range of 0–20mA (AD2700 & AD2701), ±10mA (AD2702). ▶▶▶

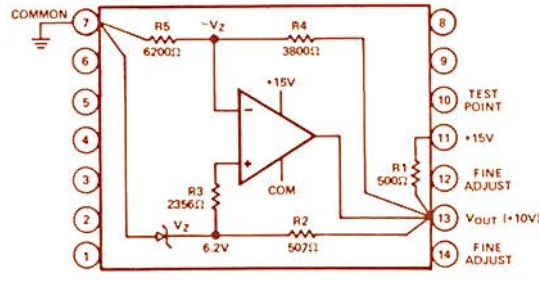


Figure 1. Basic circuit of the AD2700, showing external connection of 14-pin DIP.

‡Closer adjustment is possible with a 10kΩ pot between the trim terminals, wiper to common (AD2700). Tempco sensitivity is only 4μV/°C/mV.

FET-INPUT IC ELECTROMETERS

AD515L Op Amp Has I_b < 75fA, E_{os} < 1mV, Low Price, Guarded Inputs, Low Dissipation, Internal Compensation

by Dave Kress

The AD515J/K/L* are a family of FET-input electrometer op amps in the hermetically-sealed TO-99 package with an external guard connection. Maximum bias current (+25°C) is exceptionally low (75fA for AD515L, 150fA (K), 300fA (J)). In addition, laser-trimming and a thermally-balanced chip layout minimize offset voltage (1mV *max*. K & L) and drift (15μV/°C *max*, K, 25μV/°C *max*, L). Voltage noise is also low (4μV p-p, 0.1 to 10Hz). Prices are low ($16/$21/$27 – J/K/L, 1–24), and even lower in 100's ($9.90/$14/$18).

The AD515 is internally compensated, free from latchup, and short-circuit protected. Quiescent current with ±15V supplies is only 1.5mA, dropping to 0.5mA with ±5V supplies, making the AD515 ideal for remote battery-powered precision instruments. The J/K/L versions are specified for 0°C to +70°C operation; a new "S" version* covers the full "military" temperature range.

The maximum I_b specification is immediately usable, since it applies to units that are fully-warmed-up on ±15V supplies with no heat sink at room temperature – and the *worse* of the two inputs, at that! While the 1mV offset spec (typically 0.5mV) is low enough for many applications, it also means that for applications in which tweaking is needed, the worst-case degradation of offset tempco caused by the adjustment is less than 3μV/°C. The low power drain is not only useful in energy conservation for *continuous* battery-powering; it also keeps the effects of self-heating to a minimum for no-warmup *switched* applications, since the temperature rise is less than 10°C.

Figure 1 shows that the amplifier noise is generally lower than the Johnson noise of high-resistance sources, hence often negligible. The case can be driven (pin 8), providing shielding and guarding against noise and leakage, plus further reduction of the already-low (0.8pF) common-mode capacitance, together with the capacitance of attached input cables. Since stray capacitance is usually the ultimate limiting factor on speed in electrometer applications, this is one more benefit of the AD515. Also, it will stably drive a 1000pF output load (again helpful in remote applications). Finally, the $10^{15}\Omega$ common-mode input impedance (a result of internal bootstrapping) makes the bias current essentially independent of common-mode voltage.

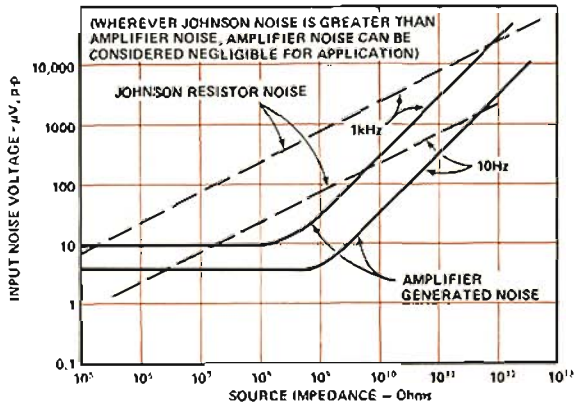


Figure 1. Peak-to-peak input noise voltage versus source impedance and bandwidth.

*Use the reply card for technical data on the AD515J/K/L and/or AD515S.

The AD515 is an obvious choice for electrometers, high-impedance buffers, long-term integrators, and charge amplifiers. Typical instrumentation systems that would benefit include photocurrent detectors, vacuum ion-gage measurement, pH/pIon electrodes, very-low-current oxygen sensors, and high-impedance biological microprobes. Its "universal" op-amp connections allow it to be simply plugged-in to upgrade performance in existing sockets employing lower-performance IC FET-input amplifiers, at little or no increase in cost.

Figures 2 and 3 show two examples of AD515 applications. In Figure 2, it is used as a very-high-impedance non-inverting amplifier. R_p is a protective resistor to limit the input fault current to 0.5mA in the event that voltages in excess of V_S are applied to the inputs, for example, if a sensor is shorted to its high-voltage bias source. The data sheet* discusses the detailed requirements for implementing guard circuits.

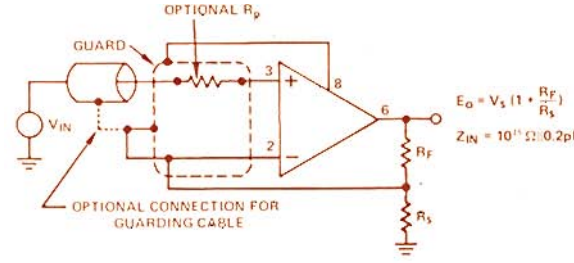


Figure 2. Very high impedance non-inverting amplifier.

In Figure 3, the AD515 is used in conjunction with an AD521† instrumentation amplifier to provide moderate bias voltage to a grounded sensor for low-current measurement, with the output again returned to ground. For high voltage, an isolation amplifier, such as Analog Devices Model 275†, might be used with the AD515.

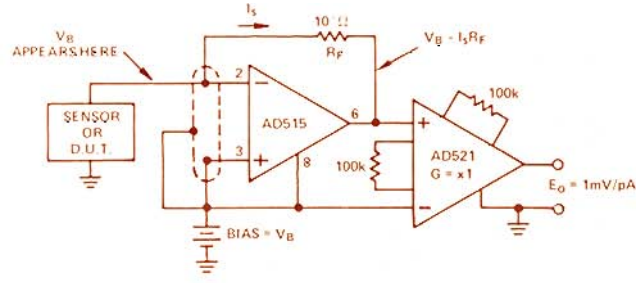
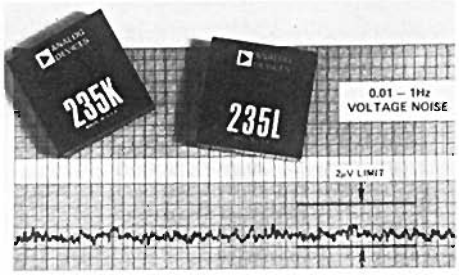


Figure 3. Current-to-voltage converter with grounded bias and sensor.

†For information on these devices, use the reply card.

LOW-COST CHOPPER

Drift < 5μV/yr
Noise < 0.5μVp-p



"It doesn't do anything new – *it just does it better*" sums up the cost-effective performance of the 235 family.

The 235J/K/L* are chopper-stabilized inverting operational amplifiers that represent a 3:1 improvement in noise (0.5μV p-p typ, 2μV p-p *max* (K, L), vs. 1.5μV p-p typ), over the predecessor 230 family. In addition, the 235 has a lower-profile package (12.7mm – 0.5" vs. 16mm – 0.62"), yet fits the same pin configuration, and has a 56% lower price ($46 vs. $105 – J, 1–9).

In addition to the low noise, voltage drift is as low as ±0.1μV/°C *max* (L), and 5μV/year, with a maximum bias-current drift of 0.5pA/°C (K, L). This combination of low noise and low drift makes the 235 ideal for such demanding applications as weighing instruments that require high accuracy and excellent long-term stability without the use of "front-panel" balance potentiometers or periodic internal adjustment.

Typical applications include amplification of microvolt-level signals, precision integration, analog computing, and preamplification in high-precision low-frequency applications, such as DVM's, 12 – 16-bit A/D converters, and error amplifiers in servo- and null-detection measurement systems.

Specs of the 3 versions (J/K/L) include *max* initial offset voltage: ±25μV/±25μV/±15μV, *max* drift: ±0.5μV/°C, ±0.25μV/°C, ±0.1μV/°C, *max* bias current: ±100pA/±50pA/±50pA, and *max* bias-current drift: 1pA/°C, 0.5pA/°C, 0.5pA/°C. Prices (1–9) are $46/$52/$69. ▶▶▶

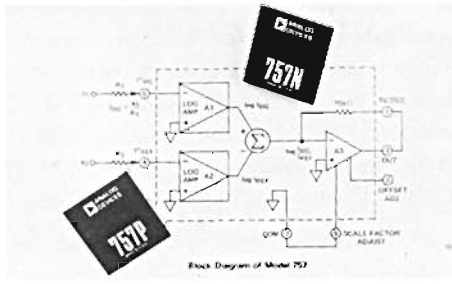
*Use the reply card for data on the 235's.

6-DECADE LOG RATIO

±0.5% Log Conformity from 10nA to 100μA
Inputs Have Symmetrical Dynamic Ranges

Model 757* is a complete temperature-compensated direct-coupled log-ratio module that spans 6 decades of dynamic range and maintains log conformity to within ±0.5% *max*, referred to the *input*, from 10nA to 100μA. Available in two versions (P/N) to handle either polarity of input, the 757 maintains log conformity of 1% r.t.i. over the entire 6-decade range (1nA to 1mA) on either input.

Unlike earlier designs, Model 757's symmetrical FET-inputs, with bias currents below 10pA, allow either input to be operated within the specified dynamic range, regardless of the signal level at the other channel. Both amplifier summing junctions are available, for either current or voltage inputs, with less than ±1mV *max* input offset voltage, a useful property when the inputs are photodiodes



operating in the short-circuit current mode, since no additional input circuitry is needed.

Drifts of scale factor and output offset are low (±0.04%/°C *max* and ±0.3mV/°C). The scale factor may be adjusted for values greater than 1V/decade, and the ±10mV *max* output offset may be zeroed simply. The 757 is housed in a 38 x 38 x 10mm (1½" x 1½" x 0.4") module and priced at $69 (1–9).

*Use the reply card for data on the 757. ▶▶▶

100kHz V/f CONVERTERS

452 Family: Linear to Within 0.015% (max)
50ppm/°C, ±30μV/°C, Prices from $39 (1-9)

Model 452J/K/L* is a family of voltage-to-frequency converters with 0.015% *max* nonlinearity and a full-scale output range of 100kHz. It is the latest addition to the line of V/f converters introduced in *Analog Dialogue* 9-3. Like the 10kHz converters described earlier*, the 452 is pin-compatible with a number of competitive 100kHz models, but at lower cost and in a smaller (38 x 38 x 10mm, 1½" x 1½" x 0.4") package, and at prices from $39 (1–9).

100kHz converters offer the designer a tenfold advantage over 10kHz devices, in either speed or resolution for the same measuring interval. The 452's offer a choice of either voltage or current inputs, with less than 150ppm (FS) nonlinearity error from 100μV to 11V, or 5nA to

0.55mA (including a 10% overrange). In A/D conversion, 16-bit-or-better resolution is available, with 12-bit accuracy and no missing codes over the whole 0° to +70°C operating range.

Three versions (J/K/L) provide a selection of price and maximum drift error (ppm of full-scale per degree C): 150/100/50, at prices of $39/$49/$59 (1–9).

*Use the reply card for technical data on the 452's, and/or 10kHz converters. ▶▶▶

THREE MORE "2nd GENERATION" DPM's

Line-Powered AD2016 (3 1/2 Digits) and AD2025 (4 3/4 Digits)
Logic-Powered AD2028 (4 3/4 Digits)

In the last issue of *Analog Dialogue* (9-2), we talked about how recent advances in technology had led us to the design of a complete line of "second-generation" digital panel meters and the benefits with which this new technology had endowed them. In the same breath, we had announced the availability of three products in this new line: The AD2021* (3½ digits, logic-powered), the AD2024* (4½ digits, line-powered), and the AD2027* (4½ digits, logic-powered).

Now, three additional "2nd-generation" DPM's are available. The six products together cover almost every popular dc application. The newcomers are:

- AD2016: 3½ digits, line powered*
- AD2025: 4¾ digits, line powered*
- AD2028: 4¾ digits, logic powered*

AD2016: 2nd GENERATION/2nd SOURCE

In designing the AD2016, the ac-line-powered "big brother" of the AD2021, we intended it to fit the pinout and generous package of the first-generation AD2009. This permits the user of the AD2009 (or any of its "second-source" competition) to use the AD2016 interchangeably, with the choice of either the gas-discharge (Beckman) display of the AD2009 or the large (13mm, 0.5") LED display of the AD2016.

The larger package size of the AD2016 gave us another advantage: the ability to provide a low-cost parallel-BCD data-output option. Space is available on the main card of the AD2016 to insert 5 logic IC's to provide the conversion from the standard character-serial BCD output to full parallel BCD data. By avoiding the cost of an additional card and its interconnections, the BCD option can be made available at small additional cost ($10, 1–9).

Another useful feature of the AD2016 is the availability of two *hold* inputs. The "converter hold" stops all conversions and holds the display unchanged; the "data hold" inhibits updating of the data outputs only, a useful feature. For example, when interfaced to a printer, the data can be held unchanged for printout, while the display output continues to follow a changing signal input. Another example might be the retention of a peak value while displaying new values.

The AD2016 measures input voltages over full-scale ranges of ±199.99mV, ±1.999V, or ±19.99V, with accuracy to within ±0.05% of reading ±0.025% of full-scale ±1 digit. A "limited differential" input is used to provide common-mode rejection at common-mode voltages within the range ±200mV. Normal-mode rejection is 40–45dB @ 50–60Hz. A new "universal" transformer permits ac power-supply specs to be changed by the user to agree with primary voltages for application worldwide. The AD2016 is priced at $128 (1–9), $138 with parallel BCD.

HIGH RESOLUTION, REASONABLE PRICE

The AD2025 and AD2028 are 4¾-digit DPM's that read up to 40,000 counts full-scale. Previously, DPM's with these higher-resolution ranges had been prohibitively expensive for many applications; second-generation circuitry now brings them within a reasonable price range. Their applications include high-resolution measurements, for example phase to 360.00°, temperature to 4000.0°, weight to 4000.0kg, as well as readings arbitrarily scaled in engineering units with adequate resolution.

The AD2025 (line powered) and the AD2028 (logic powered) measure input voltages over full-scale ranges of 3.9999V or ±39.999V with an accuracy of ±0.005% of reading ±0.005% F.S. ±1 digit. Limited differential inputs provide 50dB of CMR at up to ±200mV common-mode voltage. Normal-mode rejection is 25dB at 50–60Hz. BCD outputs are standard in a character-serial format; parallel BCD data is optional.

Since the AD2025 uses the same pin connections as the AD2024, and the AD2028 the same connections as the AD2027, the user can have the choice of either 4¾ or 4½ digits in a given application, without changing either the panel cutout or the pin connections. Prices are: AD2025, $259 (1–9); AD2028, $249 (1–9); parallel BCD (either model), $27.

▶▶▶

*Use the reply card to request specific data sheets, and/or the new 16-page *DPM Designer's Guide*.

Application Brief

SIMPLE RULES FOR CHOOSING RESISTOR VALUES IN ADDER-SUBTRACTOR CIRCUITS

by Dan Sheingold

THE PROBLEM

I want to take a linear combination of analog voltages with both positive and negative coefficients, using a single operational amplifier. In Figure 1, for example:

$$Z = 3\,x_1 + 0.15\,x_2 - 2.9\,y_1 \text{*} \qquad (1)$$

To minimize offset-current error, I want to keep the equivalent parallel resistance on both sides equal. How do I choose the nominal resistance values, given a specified value of parallel resistance, and fit within all the constraints without indulging in a lot of hairy network analysis?

In general, one must be concerned with: the effect of the resistance values on the subtractive side on gain for signals on the positive side, interaction among the inputs on the positive side, and the equal-parallel-resistance constraint. A loading resistor to ground from one of the two summing points provides a necessary degree of freedom.

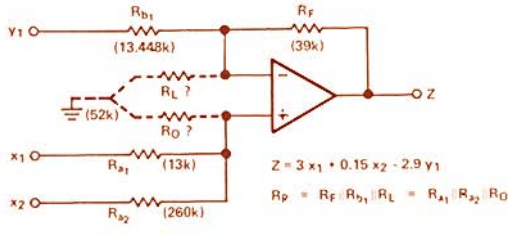


Figure 1. Typical adder-subtractor problem.

A SOLUTION[1]

This is a mechanized procedure for computing all the required values. *It works in all practical cases, for any number of inputs on either side, whether the circuit is inverting-only, non-inverting only, or an adder-subtractor, and for all reasonable values of gain or attenuation.*

Grouping the positive and negative coefficients, we label each positive coefficient a_i, the corresponding input x_i, and the corresponding input resistor R_{a_i}. Corresponding quantities for each inverted gain are b_j, y_j, and R_{b_j}. In the example of Figure 1, a_1 is 3.00, a_2 is 0.15, and b_1 is 2.90. We want to compute the values of R_{a_1}, R_{a_2}, R_{b_1}, the feedback resistance R_F, and the value and disposition (to the + or the - input?) of the grounded loading resistor (R_O or R_L), in order to keep the effective parallel resistance on both sides equal to a specified value, R_p – for example, 10kΩ.

* Expressed in general and compact form,

$$Z = \sum_{i=1}^{m} a_i x_i - \sum_{j=1}^{n} b_j y_j$$

[1] An earlier exposition of this technique by the author, with additional examples, may be found in *Electronics*, June 12, 1975, page 125.

Here are the rules:

1. *Add up the positive coefficients,* Σa.
   In this example, $\Sigma a = 3 + 0.15 = 3.15$.
2. *Add up the magnitudes of the negative coefficients,* Σb, *and add 1.00.*
   In this example, $1 + \Sigma b = 1 + 2.9 = 3.9$.
3. *Subtract* Σa *from* $(1 + \Sigma b)$ *to get the difference,* Δ. *If* Δ *is positive, a resistance* R_O *will be required between the amplifier's + input and ground; if negative, a resistance* R_L *will be required between the - input and ground.*
   In this example, $\Delta = 3.9 - 3.15 = +0.75$, calling for a resistance R_O from the + input to ground.
4. *Calculate* R_F. *It is simply equal to the product of* R_p *and the larger of the two sums.*
   In this case, since $3.9 > 3.15$, $R_F = 3.9 \times 10k\Omega = 39k\Omega$.
5. *Calculate* R_O *(or* $-R_L$*). It is equal to* R_F/Δ.
   Here, $R_O = 39k\Omega/(+0.75) = 52k\Omega$.
6. *Calculate each of the input resistances,* R_{a_i} *and* R_{b_j}. *Simply divide* R_F *by each coefficient* (a_i, b_j) *in turn.*
   In this case, $R_{a_1} = 39k\Omega/3.00 = 13k\Omega$,
   $R_{a_2} = 39k\Omega/0.15 = 260k\Omega$, and
   $R_{b_1} = 39k\Omega/2.9 = 13.448k\Omega$.

That's all, folks!

You'll find it harder to check the results from first principles than it was to execute the algorithm. The first step is to check the parallel resistances on both sides. In the example, the parallel resistance on the – side is $1/(1/39 + 1/13.448) = 10.00k\Omega$. On the + side, it is $1/(1/13 + 1/260 + 1/52) = 10.00k\Omega$. If you wish, you may satisfy yourself that the individual gain criteria are also met.

A note on implementing the circuits: Interaction among the R_{a_i} values makes dynamic trimming of the whole circuit difficult. For this reason, the resistance ratios should be trimmed *before* the network is connected to its circuit. If a final trim is needed, R_F is first tweaked to optimize overall gain accuracy for the subtracted inputs, then R_O (or R_L) for the + inputs. The amplifier's contribution to common-mode and gain errors can be minimized if it has high gain, high CMR, low E_{OS}, low I_{OS}, and low tempcos, e.g., the AD510.† If many identical networks are to be used, a cost-effective approach is to design a thin- or thick-film network, with resistors that accurately track one another with temperature and are initially set to within the required relative tolerances.† (Absolute accuracy is unnecessary.)

If many similar networks with differing gains are to be designed, the Reader may be interested in an HP-25 program that will provide fast and accurate implementation of the above procedure for up to 3 inputs on each side. It appears on page 18. ▶▶▶

†For information on the AD510 and custom R-networks, use reply card.

D/A CONVERSION WITH SINGLE-SUPPLY CIRCUIT

AD7520 in Current-Loop Application

by Vernon R. Clark

In computerized process-control systems, digital-to-analog converters are typically used to manipulate set-points and operate valves. General-purpose DAC's, such as the low-cost CMOS AD7520 10-bit multiplying DAC,* usually involve inverting op amps, which call for dual power supplies. However, one-sided supplies are highly desirable because of their lower cost, better reliability, and their compatibility with the 4–20mA range used in transmission of electrical control signals in process-control systems.

The single-supply scheme of Figure 1 employs the AD7520,* with an LM324 single-supply quad op amp, and an AD2700 precision 10V reference,* to provide a jumper-selected choice of two output voltage ranges, 0–10V and 2–10V. The latter range can be directly transduced into 4–20mA and 10–50mA current ranges appropriate for control systems, by schemes such as that shown.

In the circuit of Figure 1, the +24V supply is tapped at +5V for TTL logic levels. The AD2700 reference develops a precise 10 volts without needing adjustment. It is stepped down to +3V and +2V, which appear at the outputs of followers A2 and A1. The 2V output of A1 becomes the reference-ground level for the AD7520 DAC, the inverting op amp, A3, and the two 74C904 Hex Non-Inverting Buffers, which drive the logic inputs of the AD7520 (10 of the 12 buffer channels are used).

The net 1V reference voltage applied to the DAC is scaled in proportion to the digital input number (N) and inverted by amplifier A3 at unity gain. The output of A3 swings from 2V to 1.001V as N varies from 0 to 1 - 2^{-10}. Depending on the jumper connections, the 0-to-full-scale output swing of A4 is either 0–10V or 2–10V. The 2–10V range (E_4 = 2 + 8N volts) can directly scale a current-transducer output, such as the one shown, for 4–20mA or 10–50mA. The actual system uses a proprietary design, capable of generating a grounded or floating source or sink current. ▶▶▶

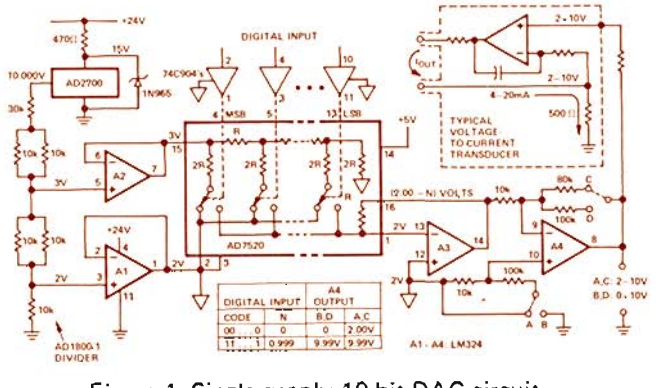


Figure 1. Single-supply 10-bit DAC circuit.

*Use the reply card for information on the AD7520, AD2700, or AD1800-1.

DIFFERENTIAL HIGH-IMPEDANCE RMS-TO-DC CONVERSION

Increased Flexibility for the 440

by Gerald W. Renken

True-rms-to-dc converters, such as Models 440 and 441*, have excellent bandwidth, accuracy, and crest-factor capability; however, their inputs are single-ended, with input impedance, typically 8.5kΩ. For use in test-equipment design, a differential-measurement capability was necessary to avoid ground-loop problems; also, it was desired that the measuring leads lightly load the circuit under test. In addition, we wanted to externally trim the overall scale factor.

The application calls for monitoring an approximately-square waveform at 20kHz, measuring its rms value to within 0.1%, and making the dc output available for measurement and control of the signal amplitude. To replace a general-purpose high-accuracy meter costing more than $1300, a 440K could be used, if it had a differential front end with impedance greater than 1MΩ.

A useful circuit approach is shown in Figure 1. The AD518, a fast-settling, low-drift op amp,* is used both for following and as a differential subtractor, to convert the differential input signal to single-ended. Though not necessary in this case, we could have reduced the probe capacitance by driving the shield with half the sum of the unity-gain follower outputs (viz., the common-mode voltage), either directly via summing resistors, or via an additional follower-connected AD518.

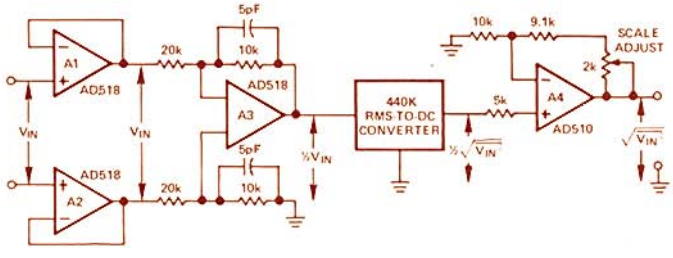


Figure 1. RMS-to-DC converter circuit with high-impedance differential input.

Gain was not necessary here; however, for low-level signals, the familiar differential instrumentation amplifier configuration (*Dialogue* 8-2, page 19) could have been used, In fact, to ensure that differential spikes could be followed (they weigh heavily in rms computation), *attenuation* was used.

Since high frequencies were involved, external filter capacitance to extend low-frequency performance (*Dialogue* 9-3, pp. 21–22) was not necessary in this application. The 440K output is followed by an amplifier stage with adjustable gain roughly equal to the preceding attenuation, to permit accurate calibration of the dc output of the overall circuit.

Extensive testing over a range of amplitudes (3–7V rms) and frequencies (5–20kHz) indicated consistent achievement of accuracy to within 0.1%. ▶▶▶

*For information on these devices, use the reply card.

Application Brief

AUDIO APPLICATION IDEAS FOR CMOS DAC'S

AD7520's Are Ideal for Signal Generation and Control

by Walter Jung

High-resolution, high-linearity multiplying DAC's that handle both polarities of analog input are naturally quite useful to the instrumentation engineer. They become equally attractive to the designer of audio signal-processing equipment when these benefits are combined with wide bandwidth and low cost.

Monolithic IC DAC's were available for some time before the advent of the 10-bit AD7520,* the 12-bit AD7521,* and the digitally-versatile AD7522,* but with generally less resolution and a limited range of reference variation. The AD7520/21/22 family lack both reference-voltage source and output amplifier, but these are not important limitations in audio use. In fact, the number-one advantage is that the reference-input voltage swing can exceed ±10V, with excellent linearity and bandwidth. Although one would expect a "multiplying DAC" to have this capability, not all types possess it fully.

Thus, not only do the 7520/7521 satisfy classical instrumentation applications with fixed unipolar references; they can also be used with bipolar voltages from volts down to millivolts. Their correct and linear ratiometric operation under such conditions makes them ideal scaling elements for audio signals. They can be viewed as digitally-programmable attenuators, which can marry high-quality audio signal-processing circuits to digitally-based systems under microprocessor control. The recently announced AD7522, with flexible storage registers, achieves interfacing with little external logic circuitry.

AUDIO PERFORMANCE OF CMOS DAC's

Besides the classical DAC specs of conversion linearity, resolution, etc., the special considerations for audio use include distortion, noise, and crosstalk in the "off" state. Interestingly enough, although they are not specifically characterized in this manner, the AD7520/21/22 come off quite well.

For instance, typical measurements of distortion are of the order of 0.05% or less over the audio band. This is due to the linearity enforced by the thin-film R-2R ladder, which ensures a linear summing-point current in the presence of a varying reference (input) voltage at a given digitally-set gain.

Noise is a parameter that can be determined from the data sheet; it is determined by the thin-film network's nominally 10kΩ characteristic resistance. This contrasts favorably with some active types of DAC's, which are noisier.

Reference-input feedthrough is specified on the data sheet as 10mV p-p (max) for 20V p-p input at 100kHz (-66dB). This, being but one point on a curve, doesn't tell the whole story. At lower frequencies, feedthrough is much less, with a floor of ≤-90dB at 1kHz (Figure 1). Feedthrough is essentially capacitively-coupled crosstalk. it is layout-sensitive.

*Use the reply card to request information on these products, or the new low-cost AD7530.

Control-signal feedthrough is undesirable in audio gain control, since it can cause thumps, pops, or clicks. Because there is no bias current in the AD7520/21/22, the output contains the desired signal current only, avoiding dc level shifts. The narrow switching spikes can be filtered without loss of bandwidth.

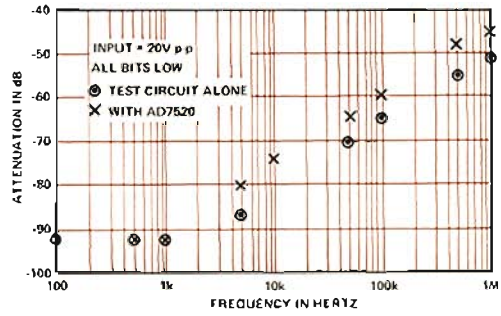


Figure 1. AD7520 feedthrough measurement.

It is interesting to consider the AD7520/21/22 accuracy in relation to the needs of audio level control. Without trim, the full-scale gain error is typically 0.3%, or, in conventional audio parlance, ±0.026dB. Even adding the loosest (conversion) nonlinearity† error, the gain error is still only ±0.043dB, adequate for a great number of audio applications, without trimming or tweaking. Remember that 1dB is close to the threshold of human perception of gain changes.

For applications where it is desirable to trim the DAC gain exactly to unity, given the possibility that it may be either high or low, resistance may be added in series with either the input (V_{REF}) terminal or the feedback terminal. Figure 2 shows a way of dealing with either contingency with one pot.

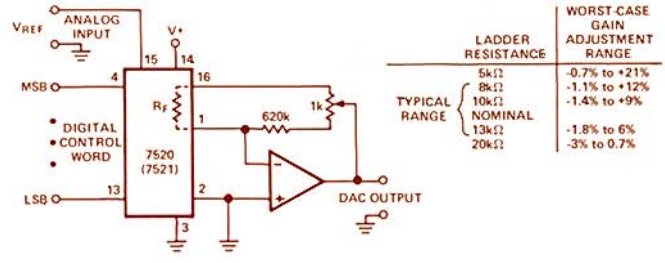


Figure 2. Single-control trim for gain calibration, allowing for a large range of absolute ladder-resistance variation.

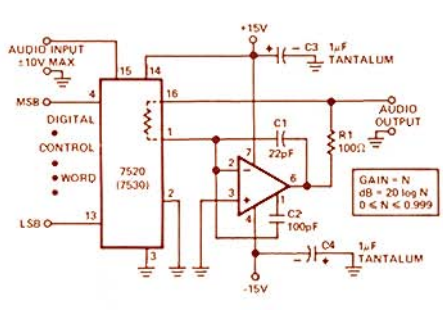
AUDIO CIRCUITS USING THE CMOS DACS (AD7520/21/22)

Figure 3 shows a basic circuit using the AD7520 as an audio gain control. A low-cost AD301A, used as the output buffer, is operated in the feedforward mode, for a gain-bandwidth of 30MHz and a 10V/μs slewing rate. This combination, using the lowest-cost "J"-suffix DAC, provides perhaps the most cost-effective, high-performance combination for an audio gain-

†Conversion-linearity errors affect only gain, not analog linearity.

control of this class. It can of course also be used as a general-purpose DAC, with device choice tailored to desired performance. Settling time to ½LSB (10 bits) is 6μs.

In general, the application of high-speed-DAC circuits to audio use can give rise to some serious problems. For instance, if the channel gain is to be manipulated while signals are present, large instantaneous gain changes in the presence of signal peaks will almost guarantee annoying audible switching-transients due to the abrupt change in level.



DIGITAL INPUTS FOR TYPICAL ATTENUATIONS

dB ATTEN.	N: INPUT NUMBER – VALUE 1 STAGE	2 STAGES
0	0.999	0.999
-1	0.891	0.944
-2	0.794	0.891
-3	0.708	0.841
-4	0.631	0.794
-5	0.562	0.750
⋮		
-10	0.316	0.562
-15	0.178	0.422
⋮		
-30	0.032	0.178
-40	0.010	0.100
-50	0.003	0.056
-60	0.001	0.032
-70	–	0.018
-80	–	0.010
-90	–	0.006

Figure 3. Inexpensive, high-performance gain control.

As a remedy, one might restrict gain-switching to times when the signal is near zero. A more-pleasing and satisfactory approach is to spread the gain change over about 50ms or more by digitally "ramping" it, using a clock and preset counter. If sufficient resolution exists, the staircase effect should be imperceptible. With an 8-bit converter, this permits 48dB of staircasing. Avoid slew-limiting in the DAC output amplifier; it can cause noxious distortion for sufficiently large gain steps, another reason for using controlled-gain steps and fast amplifiers.

Additional gain range can be obtained by cascading decade blocks of gain, or by cascading DAC's, with common digital input. If you wish to obtain the natural benefits of equal-dB gain steps, the digital number applied to the DAC(s) should vary exponentially. For m cascaded DAC's with -k dB of attenuation, the value, N, of the common digital input. should be

$$N = (10)^{k/(20m)} \qquad (1)$$

This can be achieved via software instructions in a computer system; it can also be achieved by means of programmable read-only memory (PROM), between the counter output and the DAC(s). Note that only about 2 significant digits are needed for accuracy to within 1dB, from the examples in the table (Figure 3).

Figure 4 illustrates in principle a variation of the basic gain controller which can be used to steer or "pan" an audio signal between two output channels, another common audio processing requirement. The two gains are simply made complementary. Thus, the signal will be fully *left* for all 1's, full-*right* for all 0's, and deployed equally for just the MSB on.

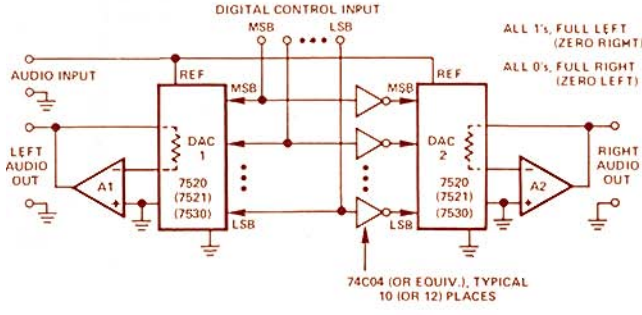


Figure 4. Digitally-programmed audio panner.

In a simpler version (Figure 5) a single DAC is used. Here, the I_{OUT2} line of a 7520, normally grounded, is used to drive a second summing amplifier with an external feedback resistor, R_{f2}. Since the current at I_{OUT2} is inherently the complement of I_{OUT1}, the circuit will work as a complementary panner. The drawback is the necessity to trim R_{f2} for equal channel gains (MSB on); since the external resistor will in general not track the network, the panner may not retain its accuracy for wide temperature variations. However, the method is simple and attractive for non-critical applications.

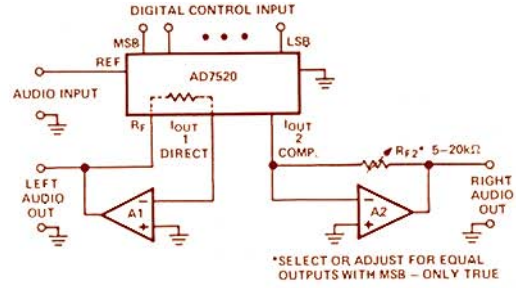


Figure 5. Simplified audio panner.

DAC's are useful for generating, as well as controlling, signals. Figure 6 shows a simple scheme for digitally programming the output frequency of a standard integrator-comparator function generator[1,2]. The timing resistor (the input resistor to the integrator) is replaced by the DAC's R-2R ladder. Since frequency is proportional to the integrator input current, it will be proportional to the digital input to the DAC.

A calibration control with wide latitude is needed because of the loose tolerance on absolute value of the R-2R ladder resistance; also, as noted above, tracking errors with temperature will limit stability. Fast amplifiers, such as the 301A (with feedforward in the integrator) are cost-effective.

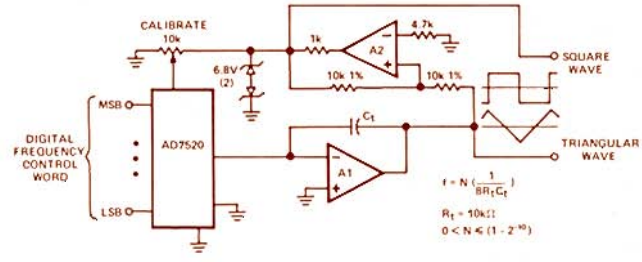


Figure 6. Programmable function generator; p-p amplitude of both waveforms is ≅15V.

There are myriad uses for these versatile DAC's; many have been documented here in the past, and more are sure to come. In audio alone, programmable oscillators, equalizers, filters, etc., may provide the Reader with food for thought.

[1] *Nonlinear Circuits Handbook*, Analog Devices, Inc., 502pp., $5.95 (soft)

[2] *Audio IC Op-Amp Applications*, W. G. Jung, Howard W. Sams & Co., Inc. Indianapolis, Indiana 46206 (soft)

Potpourri

MORE AUTHORS

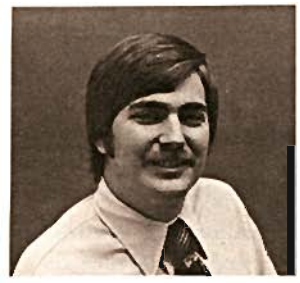
(continued from page 2)

Ivar Wold (page 3), Director of the Systems-Development Group at Analog Devices, is the inventor of the quad-slope converter. Readers of this publication became acquainted with him in *Dialogue* 7-1.

Dave Kress (pages 6 and 11) is Product Marketing Specialist at Analog Devices Semiconductor. A graduate of M.I.T. (S.B. in both Chemical and Electrical Engineering and S.M. in E.E.), he has been involved in circuit design-and-applications and wafer fabrication. Before joining ADI, he was affiliated with the Massachusetts General Hospital, where he was involved in biomedical engineering.

Dick Wagner (page 6) is Managing Engineer at Analog Devices Semiconductor. A photo and brief biography appeared in *Dialogue* 9-3.

Dennis McDonnell (page 8) is a Consultant to Analog Devices. Our readers became acquainted with him in *Dialogue* 9-2.



Jerry B. Gunn (page 10) is an Engineer at ADI's Resistor Products Division, Rochester, N.Y., designing custom thin-film resistance networks and precision hybrid voltage references. He has received an Associate EET from Illinois Central College.

Vernon R. Clark (page 15) is a project engineer involved in research and development on state-of-the-art computerized process-control systems at Applied Automation, Inc., Bartlesville, Oklahoma. Since acquiring a B.S. degree from Kansas State University, he has worked at Nortronics, Inc., General Dynamics Astronautics, and Chrysler Space Division. He is a Registered Professional Engineer and holds several patents.

Gerald Renken (page 15) is a Test-Equipment Engineer with the Government-and-Aeronautical-Products Division of Honeywell, in Minneapolis, Minnesota. He designs and develops test equipment for radar altimeters. Holding BSEE and MS degrees from the University of Illinois at Urbana, he has authored two papers.

HP-25 RESISTANCE-COMPUTATION PROGRAM FOR ADDER-SUBTRACTOR CIRCUITS

(Up to 3 Positive and Negative Terms) *See Application Brief, Page 14.*

KEYING		PROGRAM STEPS		COMMENTS
Clear program, registers, stack				
Key in 1., R/S		01	STO 1 or gNOP	STOrage steps only for coefficients that are used; See keying at 08, 13
		02	STO 2 or gNOP	
		03	STO 3 or gNOP	
		04	STO 4 or gNOP	
		05	STO 5 or gNOP	
		06	STO 6 or gNOP	
		07	CLx	
Key in non-0 coefs.	a_1, STO ÷ 1	08	R/S	Store $1/a_i$'s
	a_2, STO ÷ 2			
	a_3, STO ÷ 3			
	R/S			
		09	+	
		10	+	Sum of a_i
		11	STO 0	
		12	CLx	
Key in non-0 coefs.	b_1, STO ÷ 4	13	R/S	Store $1/b_i$'s
	b_2, STO ÷ 5			
	b_3, STO ÷ 6			
	R/S			
		14	+	
		15	+	
		16	1	
		17	+	1 + sum of b_i
		18	STO 7	
		19	RCL 0	
		20	−	Difference of sums, Δ
		21	↑	
		22	↑	
		23	g [x < 0]	(Is difference negative?)
		24	GTO 27	
		25	RCL 7	
		26	GTO 28	
		27	RCL 0	Larger of the sums
		28	R/S	
Key in R_P, R/S		29	×	$R_F = (R_P)$ (larger of sums)
		30	STO 7	
		31	$\rightleftharpoons$	
		32	g [x = 0]	Is difference (Δ) = 0?
		33	GTO 37	
		34	÷	$+R_O$ or $-R_L = R_F/\Delta$
		35	STO 0	
		36	GTO 39	
		37	0	If difference = 0, no R_O or R_L
		38	STO 0	
		39	RCL 7	(R_F)
		40	STO × 1	$R_{a1} = R_F/a_1$
		41	STO × 2	$R_{a2} = R_F/a_2$
		42	STO × 3	$R_{a3} = R_F/a_3$
		43	STO × 4	$R_{b1} = R_F/b_1$
		44	STO × 5	$R_{b2} = R_F/b_2$
		45	STO × 6	$R_{b3} = R_F/b_3$
		46	R/S	(R_F)

Contents of registers after computation

r_0	R_O or $-R_L$	r_4	R_{b1} (or R_F)
r_1	R_{a1} (or R_F)	r_5	R_{b2} (or R_F)
r_2	R_{a2} (or R_F)	r_6	R_{b3} (or R_F)
r_3	R_{a3} (or R_F)	r_7	R_F

(Zero values indicate open circuit, not zero resistance)

Walter Jung (page 16) was a design engineer at AAI Corporation in Maryland. Specializing in analog circuitry, he is involved with op amps, A/D and D/A converters, and other circuitry used in signal-processing, test-measurement, and control. A prolific writer, he has authored several books on op amps and has recently embarked on a free-lance writing career.

Book Review

Operational Amplifiers, Theory & Practice, by James K. Roberge, John Wiley & Sons, Inc., N.Y., 1975, 659 pp., xvii

The proper understanding and use of feedback is a key factor in the advancement of science and technology. The electronic operational-amplifier circuit, a microcosm representing all analog feedback systems, is perhaps the best place to learn the successful use of feedback, since the student can learn about feedback in the context of both the single "op amp" – and its related circuitry – and the use of op amps in more-complex feedback configurations, including the building of models of feedback systems occurring in other media. Experimental verification can be performed with relative ease, at low cost, and using standard electronic-laboratory equipment.

This book bids fair to become the basic text for electrical-engineering students of feedback theory and practice, amplifier circuit-design, and the design and application of operational amplifiers. It is based on a set of notes developed for the author's graduate and undergraduate students at M.I.T., and successfully serves both with a profusely-illustrated mix of theory, practice, and exercises to stimulate thinking.

The chapter headings reveal the basic structure of the book. They are: 1. Background and Objectives, 2. Properties and Modeling of Feedback Systems, 3. Linear System Response, 4. Stability, 5. Compensation [frequency], 6. Nonlinear Systems, 7. Direct-Coupled Amplifiers, 8. Operational-Amplifier Design Techniques, 9. An Illustrative Design, 10. Integrated-Circuit Operational Amplifiers, 11. Basic Applications, 12. Advanced Applications, 13. Compensation Revisited.

The treatment of these topics ranges from rather thorough and competently-presented classical amplifier and feedback theory through discussions of the consequences of the theory in practical terms, to a highly-stimulating set of "problems" for the student, at the end of each chapter. It is in these "problems" that the author raises questions that, were they to be treated in straightforward tutorial manner with the degree of thoroughness that other matters are treated, would make the volume excessively bulky and intimidating, and would probably bore the brighter students. Fully 87 pages, or 13%, of the book is given to these exercises, and this reviewer found their scope rather impressive.

The subject of compensation, and the tradeoffs between stability and bandwidth, particularly as they apply to the increased number of degrees of freedom available with externally-compensatable integrated-circuit amplifiers, receives the most comprehensive treatment this reviewer has encountered anywhere. Compensation is discussed in terms of both theory and practice, and there are a large number of illustrative oscilloscope waveforms to demonstrate the many facets of the challenging nature of optimizing response. That it is covered in two chapters, comprising 139 pages (21% of the book), may give our reader some idea of the subject's great variety, the author's thoroughness of coverage, and perhaps a key to where his strong interests lie.

On the whole, this is a (perhaps *the*) fundamental reference text on operational amplifiers; it should be on the shelves of all serious users of op amps. If it has a weakness, it may be in the area of insufficiently-detailed discussion of the broad range of applications and their implementation with commercial devices; but this is a minor weakness, since there are (and will be) many other texts that, building on the solid foundation this book provides, can serve to supply these lacks.

D.H.S.

▶▶▶

Worth Reading

LAST ISSUE OF *ANALOG DIALOGUE*
Volume 9 (1975), Number 3

Editor's Notes, Authors
Laser-Trimming on the Wafer, A Powerful New Tool for IC's
Have You Considered V/f Converters?
Monolithic CMOS 10-Bit Multiplying DAC with Registers
Get the Most from Precision Resistance Networks
DPM's: The Second Generation: LSI and Big LED's
New Products:
Low-Cost Sample-Hold for 12-Bit Data
High-Speed 12-Bit DAC: 150ns Settling to <0.01%
V/f Converter Family: Six New 10/20kHz Modules
True-RMS-to-DC Converter: High Accuracy, Low Cost, No Trims
IC Op Amp is Laser-Trimmed, $V_{OS} < 100\mu V$
Easy-to-Use SERDEX Subsystems for ASCII Interfacing
Application Briefs:
True Time-Average Over Varying Periods Using an IC DAC
Resistance-Ratio-to-Digital Conversion Using an IC A/D Converter
Measure RMS with Less Ripple and Short Settling Time
Potpourri: Brainstorming on DAC's, Improved 440 Specs, Erratum
Worth Reading: New Publications from ADI, GSA Contracts, Last Issue of *Dialogue*, Books Received
Advertisement: Modular (and IC) DAC's

ERRATA

Pages 10, 11: Pins 24 and 25 of the AD7522 are everywhere interchanged. LO-BYTE STROBE is 24, HIGH-BYTE STROBE is 25.

Page 20, Figure 1: Pin 1 of the AD7570 is V_{DD}; pin 22 is V_{CC}.

▶▶▶

Books published by trade publishers and others are occasionally mentioned or reviewed in these columns as a service to our readers. The review represents the opinion of the reviewer and is not necessarily endorsed by Analog Devices, Inc. Unless noted otherwise, these books are not available from Analog Devices, Inc.

Analog Devices introduces less of a DPM.

When we designed our new line of second generation digital panel meters, we had a clear objective in mind.

Give our customers less of everything. Less of everything they don't want in DPMs, and more of what they need.

Less confusion.

Like less confusion finding the exact DPM they require. With six different second generation DPMs (three +5VDC logic-powered and three AC line-powered) we have the biggest selection available. And each of them benefits from advanced MOS/LSI circuitry, 3½, 4½ or 4¾ digit large LED displays, a full week of failure-free, power cycled burn-in, lower power consumption and lower cost.

Less components.

But let's not talk in generalities. Let's talk specific Analog Devices DPMs where less is a plus. Take our 3½ digit 5VDC Model AD2021 for example. Through the use of MOS/LSI circuitry, we've been able to cut the number of components in it by 42%. And in doing so, chopped power consumption by 42%. Decreased the number of interconnections adding to reliability. Reduced its size to 3"W x 1.8"H x 1.25"D. And dropped its weight to 4 ounces. That's why logic power is your logical choice for compact instrumentation. Our line-powered version, AD2016, offers similar advantages, in its industry-accepted AC-powered package.

Less difficult to read.

Digital panel meters should be easy to read. Get a glimpse of our logic-powered 4¾ digit AD2028 and line-powered AD-2025. Like our other second generation Analog Devices DPMs, they have displays featuring big, high-intensity "light-pipe" LEDs almost twice the size of earlier ones.

Less cost.

With so much that's improved, you'd expect to pay more for our latest DPMs. Surprisingly, that's not the case. Our logic-powered 4½ digit Model AD2027 and line-powered Model AD2024, for instance, are priced 40% lower than their first generation predecessors.

Less is more.

When is less more? When you specify Analog Devices new line of second generation digital panel meters. The real company for precision measurement and control. For complete facts, get the Designers Guide to DPMs. Analog Devices, P.O. Box 280, Norwood, Mass. 02062.

ANALOG DEVICES

The real DPM company.

East Coast: (617) 329-4700, Midwest: (312) 894-3300, West Coast: (213) 595-1783, Texas: (214) 231-5094. Belgium: 03 38 27 07, Denmark: 97 95 99, England: 01/94 10 46 6, France: 686-77 60, Germany: 089/53 03 19, Japan: 03/26 36 82 6, Netherlands: 076-122555 and representatives around the world.

For information on specific DPMs and/or to receive your copy of the Designer's Guide, use the reply card.